

WHAT IS CLAIMED IS:

- 1 1. A capacitor comprising:
  - 2 an insulating layer overlying a substrate;
  - 3 a semiconductor layer overlying the insulator layer;
  - 4 a bottom electrode formed in a portion of the semiconductor layer;
  - 5 a capacitor dielectric overlying the bottom electrode, the capacitor dielectric comprising a
  - 6 high permittivity dielectric having a dielectric constant greater than about 5; and
  - 7 a top electrode overlying the capacitor dielectric.
- 1 2. The capacitor of claim 1 wherein the capacitor is a decoupling capacitor.
- 1 3. The capacitor of claim 2 wherein the top electrode is connected to a power supply line
- 2 and the bottom electrode is connected to a ground line.
- 1 4. The capacitor of claim 2 wherein the top electrode is connected to a first power supply
- 2 line and the bottom electrode is connected to a second power supply line.
- 1 5. The capacitor of claim 1 wherein the bottom electrode or the top electrode is substantially
- 2 flat.
- 1 6. The capacitor of claim 1 wherein the top electrode comprises poly-crystalline silicon.
- 1 7. The capacitor of claim 1 wherein the top electrode comprises a metal selected from the
- 2 group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

1 8. The capacitor of claim 1 wherein the top electrode comprises a metal nitride selected  
2 from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum  
3 nitride, or combinations thereof.

1 9. The capacitor of claim 1 wherein the top electrode comprises a metal silicide selected  
2 from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide,  
3 tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

1 10. The capacitor of claim 1 wherein the top electrode comprises a metal oxide selected from  
2 the group consisting of ruthenium oxide, indium tin oxide, or combinations thereof.

1 11. The capacitor of claim 1 wherein the high permittivity dielectric comprises hafnium  
2 oxide.

1 12. The capacitor of claim 1 wherein the high permittivity dielectric comprises a material is  
2 selected from the group consisting of aluminum oxide, hafnium oxynitride, hafnium silicate,  
3 zirconium oxide, zirconium oxynitride, zirconium silicate, or combinations thereof.

1 13. The capacitor of claim 1 wherein the high permittivity dielectric has a relative  
2 permittivity of greater than about 10.

1 14. The capacitor of claim 1 wherein the high permittivity dielectric has a relative  
2 permittivity of greater than about 20.

1 15. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of less  
2 than about 100 angstroms.

1 16. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of less  
2 than about 20 angstroms.

1 17. The capacitor of claim 1 wherein the capacitor has a width of larger than about 5  
2 microns.

1 18. The capacitor of claim 1 wherein the capacitor has a width of larger than about 10  
2 microns.

1 19. The capacitor of claim 1 wherein the capacitor has a length of larger than about 1 micron.

1 20. The capacitor of claim 1 wherein the capacitor has a length of larger than about 5  
2 microns.

1 21. The capacitor of claim 1 wherein the bottom electrode contact region is doped to the first  
2 conductivity type and wherein the bottom electrode is doped to a second conductivity type and  
3 coupled to a supply voltage that creates an inversion region of the first conductivity type.

1 22. The capacitor of claim 1 wherein the bottom electrode and the bottom electrode contact  
2 region are doped to the first conductivity type.

1 23. A decoupling capacitor comprising:

2 a semiconductor substrate comprising a silicon surface layer;

3 a substantially flat bottom electrode formed in a portion of the semiconductor surface

4 layer;

5 a capacitor dielectric overlying the bottom electrode, the capacitor dielectric comprising a

6 high permittivity dielectric with a relative permittivity greater than about 5;

7 a substantially flat top electrode overlying the capacitor dielectric; and

8 wherein the top electrode is electrically coupled to a first reference voltage line and the

9 bottom electrode is electrically coupled to a second reference voltage line.

1 24. The capacitor of claim 23 wherein the top electrode is connected to a power supply line

2 and the bottom electrode is connected to a ground line.

1 25. The capacitor of claim 23 wherein the top electrode is connected to a first power supply

2 line and the bottom electrode is connected to a second power supply line.

1 26. The capacitor of claim 23 wherein the semiconductor substrate is a bulk silicon substrate.

1 27. The capacitor of claim 23 wherein the semiconductor substrate is a silicon-on-insulator

2 substrate.

1 28. The capacitor of claim 23 wherein the top electrode comprises silicon.

1 29. The capacitor of claim 23 wherein the top electrode comprises a metal selected from the

2 group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

1 30. The capacitor of claim 23 wherein the top electrode comprises a metal nitride selected  
2 from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum  
3 nitride, or combinations thereof.

1 31. The capacitor of claim 23 wherein the top electrode comprises a metal silicide selected  
2 from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide,  
3 tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

1 32. The capacitor of claim 23 wherein the high permittivity dielectric comprises hafnium  
2 oxide.

1 33. The capacitor of claim 23 wherein the high permittivity dielectric comprises a material  
2 selected from the group consisting of hafnium oxynitride, hafnium silicate, zirconium oxide,  
3 zirconium oxynitride, zirconium silicate, and combinations thereof.

1 34. The capacitor of claim 23 wherein the high permittivity dielectric has a relative  
2 permittivity of greater than 10.

1 35. The capacitor of claim 23 wherein the high permittivity dielectric has a relative  
2 permittivity of greater than 20.

1 36. The capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less  
2 than about 100 angstroms.

1 37. The capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less  
2 than about 50 angstroms.

1 38. The capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less  
2 than about 10 angstroms.

1 39. The capacitor of claim 23 wherein the capacitor has a width of larger than about 5  
2 microns.

1 40. The capacitor of claim 23 wherein the capacitor has a width of larger than about 10  
2 microns.

1 41. The capacitor of claim 23 wherein the capacitor has a length of larger than about 1  
2 micron.

1 42. The capacitor of claim 23 wherein the capacitor has a length of larger than about 5  
2 microns.

1 43. The capacitor of claim 23 wherein the bottom electrode is doped to a first conductivity  
2 type, the capacitor further comprising adjacent doped regions doped to a second conductivity  
3 type.

1 44. The capacitor of claim 43 wherein the first conductivity type is n-type and the second  
2 conductivity type is p-type.

1 45. The capacitor of claim 43 wherein the first conductivity type is p-type and the second  
2 conductivity type is n-type.

1 46. The capacitor of claim 23 wherein the bottom electrode is doped to a first conductivity  
2 type, the capacitor further comprising adjacent doped regions with the first conductivity type.

1 47. The capacitor of claim 23 and further comprising spacers formed on sides of the top  
2 electrode.

1 48. The capacitor of claim 47 and further comprising an etch-stop layer overlying the top  
2 electrode and the spacers.

1 49. The capacitor of claim 48 wherein the etch-stop layer comprises silicon nitride.

1 50. The capacitor of claim 48 and further comprising an inter-layer dielectric overlying the  
2 etch-stop layer.

1 51. The capacitor of claim 50 wherein the inter-layer dielectric comprises silicon oxide.

1 52. The capacitor of claim 50 wherein the inter-layer dielectric comprises a dielectric with a  
2 relative permittivity less than about 3.5.

1 53. The capacitor of claim 50 wherein the inter-layer dielectric comprises a dielectric with a  
2 relative permittivity less than about 3.0.

1 54. The capacitor of claim 50 wherein the inter-layer dielectric is selected from the group  
2 consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen  
3 silsesquioxane (HSQ), and SiOF.

1 55. The capacitor of claim 50 and further comprising a first contact plug in electrical contact  
2 with the bottom electrode and a second contact plug in electrical contact with the top electrode.

1 56. The capacitor of claim 23 further comprising a shallow trench isolation region adjacent to  
2 the bottom electrode.

1 57. The capacitor of claim 23 wherein semiconductor substrate comprises a semiconductor  
2 on insulator substrate including a plurality of islands, wherein the islands are isolated from one  
3 another by mesa isolation.

1 58. A method of forming a capacitor, the method comprising:  
2 providing a silicon-on-insulator substrate including a silicon layer overlying an insulator  
3 layer;  
4 forming a bottom electrode in the silicon layer;  
5 forming a capacitor dielectric on bottom electrode, the capacitor dielectric comprising a  
6 high permittivity dielectric with a relative permittivity greater than about 5;  
7 forming a top electrode on capacitor dielectric;  
8 forming a bottom electrode contact region within the strained silicon layer adjacent the  
9 bottom electrode; and  
10 electrically connecting the bottom electrode and the bottom electrode contact region.

1 59. The method of claim 58 wherein the capacitor is a decoupling capacitor.

1 60. The method of claim 58 wherein the step of forming the bottom electrode comprises:  
2 forming an active region;  
3 forming isolation regions surrounding the active region; and  
4 doping the active region.

1 61. The method of claim 60 wherein the active region has a doping concentration of greater  
2 than about  $10^{19}\text{cm}^{-3}$ .

1 62. The method of claim 58 wherein forming the capacitor dielectric comprises a chemical  
2 vapor deposition step.

1 63. The method of claim 58 wherein forming the capacitor dielectric comprises a sputtering  
2 deposition step.

1 64. The method of claim 58 wherein the step of forming the capacitor dielectric comprises:  
2 forming an interfacial oxide layer; and  
3 forming a high permittivity dielectric layer.

1 65. The method of claim 58 and further comprising:  
2 doping a portion of the silicon layer not covered by top electrode;  
3 forming spacers on sides of the top electrode; and  
4 doping a portion of the silicon layer not covered by the top electrode and spacers.

1 66. The method of claim 65 wherein the spacers comprise silicon nitride.

1 67. The method of claim 65 further comprising:  
2 depositing an etch-stop layer over top electrode and spacers;  
3 forming an inter-layer dielectric over etch-stop layer;  
4 forming contact holes in inter-layer dielectric; and  
5 filling the contact holes with a conductive material to form contact plugs.

1 68. The method of claim 67 wherein the etch-stop layer comprises silicon nitride.

1 69. The method of claim 67 wherein the inter-layer dielectric comprises silicon oxide.

1 70. The method of claim 67 wherein the inter-layer dielectric comprises a dielectric with a  
2 relative permittivity less than about 3.5.

1 71. The method of claim 67 wherein the inter-layer dielectric comprises a dielectric with a  
2 relative permittivity less than about 3.0.

1 72. The method of claim 67 wherein the inter-layer dielectric is selected from the group  
2 consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen  
3 silsesquioxane (HSQ), and SiOF.

1 73. The method of claim 67 wherein the contact plugs comprise a first contact plug that  
2 electrically contacts the bottom electrode and a second contact plug that electrically contacts the  
3 top electrode.

1 74. The method of claim 73 wherein the top electrode is electrically coupled to a power  
2 supply line and the bottom electrode is electrically coupled to a ground line.

1 75. The method of claim 73 wherein the top electrode is electrically coupled to a first power  
2 supply line and the bottom electrode is electrically coupled to a second power supply line.

1 76. The method of claim 58 wherein the insulator layer comprise silicon oxide.

1 77. The method of claim 58 wherein the insulator layer has a thickness of less than about  
2 1200 angstroms.

1 78. The method of claim 58 wherein the silicon layer has a thickness of less than about 1000  
2 angstroms.

1 79. The method of claim 58 wherein the top electrode comprises silicon.

1 80. The method of claim 58 wherein the top electrode comprises a metal selected from the  
2 group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

1 81. The method of claim 58 wherein the top electrode comprises a metallic nitride selected  
2 from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum  
3 nitride, or combinations thereof.

1 82. The method of claim 58 wherein the top electrode comprises a metallic silicide selected  
2 from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide,  
3 tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

1 83. The method of claim 58 wherein the high permittivity comprises hafnium oxide.

1 84. The method of claim 58 wherein the high permittivity dielectric is selected from the  
2 group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate,  
3 zirconium oxide, zirconium oxynitride, zirconium silicate, or combinations thereof.

1 85. The method of claim 58 wherein the high permittivity dielectric has a relative  
2 permittivity of greater than about 10.

1 86. The method of claim 58 wherein the high permittivity dielectric has a relative  
2 permittivity of greater than about 20.

1 87. The method of claim 58 wherein the capacitor dielectric has a physical thickness of less  
2 than about 100 angstroms.

1 88. The method of claim 58 wherein the capacitor dielectric has a physical thickness of less  
2 than about 50 angstroms.

1 89. The method of claim 58 wherein the capacitor dielectric has a physical thickness of less  
2 than about 10 angstroms.

1 90. The method of claim 58 wherein the capacitor has a width of greater than about 5  
2 microns.

1 91. The method of claim 58 wherein the capacitor has a width of greater than about 10  
2 microns.

1 92. The method of claim 58 wherein the capacitor has a length of greater than about 1  
2 micron.

1 93. The method of claim 58 wherein the capacitor has a length of greater than about 5  
2 microns.